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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,452	ELLSBERRY ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on August 23, 2004 has been received and entered in the case.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: on page 14, line 8 of the specification refers to a plurality of underside electrical interconnects "508" which is not referenced in the figures. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly

labeled as "Annotated Marked-up Drawings" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Since applicant has not responded or amended to the objection in the above paragraph, the objection is maintained.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 6, 8, 9, 11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelly et al. (U. S. Pat. No. 5,798,567).

Regarding claim 1, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 a chip-scale package comprising:

- a substrate (43) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

- a memory die (41) mounted on the first surface of the substrate using a plurality of rigid underside coupling members (45), the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the memory die;
- a plurality of solder balls (49) mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder balls electrically coupled to at least one of the underside coupling members;
- a plurality of pads (the pads under the element 47) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and
- one or more electronic components (47) mounted on the second surface of the substrate in an area substantially opposite of the memory die, wherein the combined distance that an electronic component and the memory die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

Regarding claim 2, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 electrically conductive traces on the first surface to electrically couple at least one solder ball to the memory die.

Regarding claim 3, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 the substrate (43) including a controlled thermal expansion material that "sufficiently" matches the coefficient of expansion of the memory die.

Regarding claim 4, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 – 31 the underside coupling members (45) permit the underside surface of the memory die to be substantially exposed.

Regarding claim 5, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 a chip-scale package comprising:

- a substrate (43) having a first surface and an opposite second surface;
- a semiconductor device (41) mounted on the first surface of the substrate using solder balls;
- a plurality of solder balls (49) mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder balls electrically coupled to the semiconductor device;
- a plurality of pads (the pads under the element 47) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and
- one or more electrical components (47) mounted on the second surface of the substrate.

Regarding claim 6, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 the electrical components (47) being mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device.

Regarding claim 8, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 the combined distance that an electrical component and the semiconductor device protrude from the substrate being less than the distance that a solder ball and pad protrude from the substrate.

Regarding claim 9, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 the substrate (43) including a controlled thermal expansion material with a coefficient of expansion that substantially matches the coefficient of expansion of the semiconductor device.

Regarding claim 11, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 electrically conductive traces on the first surface to electrically couple at least one solder ball to the semiconductor device.

Regarding claim 13, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 the semiconductor device (41) being coupled to the first surface using rigid underside coupling members (45).

Regarding claim 14, Kelly et al. discloses in e.g., Fig. 4 and column 3, lines 23 - 31 the rigid underside coupling members (45) permitting the underside surface of the semiconductor device to be substantially exposed.

6. Claims 1 – 9, 11, and 13 – 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (U. S. Pat. No. 6,597,062).

Regarding claim 1, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 a chip-scale package comprising:

- a substrate (52) having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material (column 7, lines 8 - 21);
- a memory die (54a) mounted on the first surface of the substrate using a plurality of rigid underside coupling members (pads under the elements 54a), the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the memory die (column 7, lines 8 - 21);
- a plurality of solder balls (the solder balls in the 62a and 62b) mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder

balls electrically coupled to at least one of the underside coupling members (column 7, lines 50 - 62);

- a plurality of pads (the pads under the elements 64a, 64b and 54b) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and
- one or more electronic components (the elements 60 and 58 that are located at the same side as the element 54b) mounted on the second surface of the substrate in an area "substantially" opposite of the memory die, wherein the combined distance that an electronic component and the memory die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate (column 7, lines 25 - 40).

Regarding claim 2, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 electrically conductive traces on the first surface to electrically couple at least one solder ball to the memory die (column 7, lines 50 - 62).

Regarding claim 3, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the substrate (52) including a controlled thermal expansion material that "sufficiently" matches the coefficient of expansion of the memory die.

Regarding claims 4, 14, 19 and 26, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the rigid underside coupling members (the pads under the elements 54a) permitting the underside surface of the semiconductor device to be substantially exposed.

Regarding claim 5, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 a chip-scale package comprising:

- a substrate (52) having a first surface and an opposite second surface;
- a semiconductor device (54a) mounted on the first surface of the substrate using solder balls;
- a plurality of solder balls (since the elements 54a is BGA, column 6, line 51, the solder balls under the 54a) mounted on the first surface of the substrate in a ball grid array configuration, at least one of the solder balls electrically coupled to the semiconductor device (column 7, lines 50 - 62);
- a plurality of pads (the pads under the elements 64a, 64b and 54b) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and
- one or more electrical components (the elements 60 and 58 that are located at the same side as the element 54b) mounted on the second surface of the substrate.

Regarding claim 6, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the electrical components (the elements 60 and 58 that are located at the same side as the element 54b) being mounted on the second surface of the substrate in an area "substantially" opposite of the semiconductor device.

Regarding claim 7, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the electrical components (the elements 60 and 58 that are located at the same side as the element 54b) including capacitors and resistors.

Regarding claim 8, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the combined distance that an electrical component and the semiconductor

device protrude from the substrate being less than the distance that a solder ball and pad protrude from the substrate.

Regarding claim 9, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the substrate (52) including a controlled thermal expansion material with a coefficient of expansion that substantially matches the coefficient of expansion of the semiconductor device.

Regarding claim 11, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 electrically conductive traces on the first surface to electrically couple at least one solder ball to the semiconductor device.

Regarding claim 13, Li et al. discloses in e.g., Figs. 2a – 2c and column 6, line 36 – column 10, line 24 the semiconductor device (54a) being coupled to the first surface using rigid underside coupling members (the pads under the elements 54a).

Regarding claim 15, the claim further requires a stackable electronic assembly that comprising:

- a plurality of chip-scale packages.

Li et al. clearly shows in Fig. 3a a plurality of chip-scale packages (51a -c), the plurality of chip-scale packages arranged in a stacked configuration, each chip-scale package including (see rejection under claim 5) and wherein the combined distance that an electronic component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate (See Fig. 3a).

Regarding claim 16, Li et al. discloses in e.g., Fig. 3b the plurality chip-scale packages having identical routing traces.

Regarding claim 17, Li et al. discloses in e.g., Figs. 3a and 3b the solder balls on the first surface of a first chip-scale package being coupled to the pads on the second surface of a second chip-scale package.

Regarding claim 18, Li et al. discloses in e.g., Figs. 3a and 3b the staggered routing scheme permits accessing the same underside coupling member in each of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package.

Regarding claim 20, the claim further requires a memory module that comprising: a main substrate and one or more stacks of memory devices coupled to a first surface of the main substrate.

Li et al. clearly shows in Fig. 3a

- a main substrate (12) with an interface to couple the memory module to other devices; and
- one or more stacks of memory devices (51a - c) coupled to a first surface of the main substrate,
    - o at least one stack of memory devices including (see rejection under claim 5).

Regarding claim 21, Li et al. discloses in e.g., Figs. 3a and column 10, line 25 – column 11, line 8

- the substrate (52) is composed of a controlled thermal expansion material, the substrate has a coefficient of expansion that substantially matches a coefficient of expansion of the memory semiconductor die (54a),
- the plurality of solder balls (the solder balls in the elements 62a and 62b) are mounted on the first surface of the substrate in a ball grid array configuration, and

- each chip-scale package further includes
    - a plurality of pads (the pads under the elements 54b, 64a and 64b) coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme, and
    - one or more electronic components (the elements 60 and 58 that are located at the same side as the element 54b) mounted on the second surface of the substrate in an area "substantially" opposite of the memory semiconductor die, wherein the combined distance that an electronic component and the memory semiconductor die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

Regarding claim 22, Li et al. discloses in e.g., Figs. 3a and 3b the staggered routing scheme permitting accessing the same underside coupling members in all of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package.

Regarding claim 23, Li et al. discloses in e.g., Figs. 3a and 3b the memory module being a dual inline memory module.

Regarding claim 24, Li et al. discloses in e.g., Fig. 3a one or more stacks of memory devices (54b) coupled to a second surface of the main substrate.

Regarding claim 25, Li et al. discloses in e.g., Figs. 3a, 3b and column 10, line 25 – column 11, line 8 the chip-scale packages being stacked with the solder balls (since the elements 62a/62b and 64a/64b are BGA, column 7, lines 50 - 62, the solder balls are located in the 62a/62b and 64a/64b) on the first surface of a chip-scale package (51b) coupled (since the bus line 84 clearly shows the electrical connections between each one of the chip-scale packages in

the stack, the packages are physically coupled to each other's pads) to pads on the second surface of another chip-scale package (51c).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in view of Hosomi (U. S. Pat. No. 6,740,981).

Li et al. discloses the claimed invention except for the semiconductor device being a silicon memory device (claims 10 and 12) and the substrate including a controlled thermal expansion material that sufficiently matches the coefficient of expansion of the silicon device (claim 10). Hosomi teaches in e.g., Fig. 5 and column 11, lines 24 - 25 a semiconductor device (57A; silicon chip) being a silicon memory device and a substrate (1) including a controlled thermal expansion material that "sufficiently" matches the coefficient of expansion of the silicon device. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Li et al. by using silicon as the material of the die and the material of the substrate being sufficiently matches the coefficient of expansion of the silicon device as taught by Hosomi. The ordinary artisan would have been motivated to modify Li et al. in the manner described above for at least the purpose of (1) increasing heat dissipation and (2) increasing arc- and track-resistant.

Response to Arguments

9. Applicant's arguments filed on August 30, 2004 have been fully considered but they are not persuasive.

On page 13, applicant argues "Kelly et al. does not teach 'the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the memory die' as claimed." This argument is not persuasive. Since the term "substantially" is a broad term and any substrate for a die has a coefficient of expansion that "substantially matches" a coefficient of expansion of any die (e.g., a memory die), the BGA substrate of Kelly et al.'s coefficient of expansion "substantially matches" a coefficient of expansion of a memory die.

Further, applicant argues "Kelly et al. fails teach 'each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme' as claimed. In particular, the Office Action does not point to any staggered routing scheme disclosed by Kelly et al. Kelly et al. merely teaches electrical connections between solder balls (49) and electrical pads 56. However, this does not constitute a staggered routing scheme as illustrated in Figures 3 and 7 of the present application." This argument is not persuasive. Kelly et al. clearly shows in Fig. 4 each pad (the pads under the element 47) electrically coupled to one or more of the plurality of solder balls (49) in a staggered routing scheme (e.g., through 56, 55 and the pads under the solder balls 49).

Furthermore, applicant argues "Kelly et al., Col. 3, lines 23- 31, teaches the 'substrate includes a controlled thermal expansion material that sufficiently matches the coefficient of expansion of the memory die.' However, Applicants submit that Kelly et al. is silent as the thermal expansion properties of the substrate and memory die." This argument is not persuasive because the features upon which applicant relies (i.e., the thermal expansion properties of the substrate and memory die) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

Next, applicant argues "Kelly et al. teaches 'the combined distance that an electrical component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.' Applicants submit that Kelly et al. fails to teach this physical relation between the claimed components." This argument is not persuasive. Kelly et al. clearly shows in Fig. 4 that the combined distance of an electrical component (45) and the semiconductor device (41) protrude from the substrate (43) is less than the distance that a solder ball (49) and pad protrude from the substrate (43).

Next, applicant argues "Li et al. fails to teach 'each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme' as claimed." This argument is not persuasive. Li et al. clearly shows in e.g., Fig. 3b each pad (the pads under the elements 64a, 64b and 54b) electrically coupled to one or more of the plurality of solder balls (the solder balls

in the 62a and 62b) in a staggered routing scheme (see the electrical line 84 in e.g., Fig. 3b that connects the each pads to the solder balls by a staggered routing scheme).

Next, applicant argues "Applicants submit that Fig. 3b of Li et al. does not teach identical routing traces on each of the stacked configurations." This argument is not persuasive. Li et al. clearly shows in Fig. 3b that identical elements (solder balls in the 62a, 62b, 64a and 64b; the structure 54a and 54b) are located at the same locations on the substrate (52) of the each packages (51a and 51b) and the electrical communication line 84 passes same routing traces on each of the stacked package (51a and 51b). Thus, Li et al. discloses the limitation "identical routing traces (the electrical traces on the elements 51a and 51b) on each of the stacked configurations (51a and 51b)."

Finally, applicant argues "Applicants submit that Figs. 3a and 3b of Li et al. do not teach the claimed staggered routing scheme that permits accessing the same underside coupling member in all of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package as claimed and illustrated in Figures 3 and 7 (see references 71 1, 713, 717, and 719). In particular, Li et al. Fig. 3a does not teach any routing scheme and Fig. 3b only teaches a single trace (84), not a staggered routing scheme as claimed." This argument is not persuasive. The element 84 in Li et al. shows how electrical traces are connected (e.g., staggered routing between 62a and the element 54a, at the right side) between each of the stacked packages in an abstract way not an electrical connection of a single trace. Thus, Li et al. discloses in e.g., Fig. 3b staggered routing scheme (e.g., staggered routing between 62a and the element 54a, at the

right side) that permits accessing the same underside coupling member (e.g., solder balls in the 62a and 64a) in all of the chip-scale packages (e.g., 51a and 51b) in a stack from a plurality of solder balls in a first chip-scale package.

For the above reasons, the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Friday, November 05, 2004

GEORGE ECKERT
PRIMARY EXAMINER